PTO/SB/08A(08-03)

Substitute for form 1449A&B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	10/718,968
Filing Date	November 21, 2003
First Named Inventor	Baeckler
Art Unit	2819
Examiner Name	Not Yet Assigned
Attorney Docket Number	015114-093700US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
CN	AA	US-5,260,610	11-1993	Pedersen et al.	
	AB	US-5,260,611	11-1993	Cliff et al.	
	AC	US-5,274,581	12-1993	Cliff et al.	
	AD	US-5,295,090	03-1994	Hsieh et al.	
	AE	US-5,349,250	09-1994	New	
	AF	US-5,359,242	10-1994	Veenstra	
	AG	US-5,359,468	10-1994	Rhodes et al.	
	AH	US-5,365,125	11-1994	Goetting et al.	
	AI	US-5,436,575	07-1995	Pedersen et al.	
	AJ	US-5,481,206	01-1996	New et al.	
	AK	US-5,481,486	01-1996	Cliff et al.	
	AL	US-5,483,478	01-1996	Chiang	
	AM	US-5,485,103	01-1996	Pedersen et al.	
	AN	US-5,488,316	01-1996	Freeman et al.	
	AO	US-5,500,608	03-1996	Goetting et al.	
	AP	US-5,523,963	06-1996	Hsieh et al.	
	AQ	US-5,546,018	08-1996	New et al.	
	AR	US-5,629,886	05-1997	New	
	AS	US-5,631,576	05-1997	Lee et al.	
	AT	US-5,672,985	09-1997	Lee	
	AU	US-5,675,262	10-1997	Duong et al.	
	AV	US-5,724,276	03-1998	Rose et al.	
	AW	US-5,761,099	06-1998	Pedersen	
	AX	US-5,818,255	10-1998	New et al.	
	AY	US-5,889,411	03-1999	Chaudhary	
	AZ	US-5,898,319	04-1999	New	
	BA	US-5,898,602	04-1999	Rothman et al.	
	BB	US 5,909,126	06-1999	Cliff et al.	
	BC	US 5,999,016	12-1999	McClintock et al.	
	BD	US 6,021,423	02-2000	Nag et al.	
	BE	US 6,051,992	04-2000	Young et al.	
	BF	US 6,107,827	08-2000	Young et al.	
	BG	US 6,118,300	09-2000	Wittig et al.	
	BH	US 6,154,052	11-2000	New	
	BI	US 6,154,053	11-2000	New	
	BJ	US 6,154,055	11-2000	Cliff et al.	
	BK	US 6,157,209	12-2000	McGettigan	
	BL	US-6,181,610 B1	02-2001	Wittig et al.	
CN	BM	US 6,191,611 B1	02-2001	Altaf	

Examiner Signature	/Chuong Ngo/	Date Considered	02/02/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A&B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	10/718,968
Filing Date	November 21, 2003
First Named Inventor	Baeckler
Art Unit	2819
Examiner Name	Not Yet Assigned
Attorney Docket Number	015114-093700US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number: Number Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
CN	BN	US-6,288,568 B1	09-2001	Bauer et al.	
	BO	US 6,288,570 B1	09-2001	New	
	BP	US 6,297,665 B1	10-2001	Bauer et al.	
	BQ	US 6,323,682 B1	11-2001	Bauer et al.	
	BR	US 6,400,180 B2	06-2002	Wittig et al.	
CN	BS	US 6,501,296 B2	12-2002	Wittig et al.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
CN	BT	AHMED, Elias et al.; "The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density"; 2000, FPGA, pp. 3-12.	
	BU	BAECKLER, Gregg; "Altera Raphael Device Family: Modification to Scheme 7 for Adding 3 numbers"; 2002, 14 pages.	
	BV	CHEREPACHA, Don et al.; "DP-FPGA Architecture Optimized for Datapaths"; 1996, VLSI Design, Vol. 4, No. 4, pp. 329-343.	
	BW	KAPTANOGLU, Sinan et al.; "A new high density and very low cost reprogrammable FPGA architecture"; 1999, FPGA, pp. 3-12.	
	BX	KOULOHERIS, Jack L. et al.; "FPGA Area versus Cell Granularity - Lookup Tables and PLA Cells"; 1992, FPGA, pp. 9-14.	
	BY	ROSE, Jonathan et al.; "Architecture of Field-Programmable Gate Arrays: The Effect of Logic Block Functionality on Area Efficiency"; 1990, IEEE Journal of Solid-State Circuits, Vol. 25, No. 5, pp. 1217-1225.	
	BZ	"Computer Arithmetic: A.2: Basic Techniques of Integer Arithmetic, 4 pages.	
	CA	"FLEX 8000, Programmable Logic Device Family"; 1999, Altera Version 10.01, pp. 349-364.	
	CB	"FLEX 10K, Embedded Programmable Logic Device Family"; 2001, Altera Version 4.1, pp. 1-28.	
	CC	"FLEX 6000, Programmable Logic Device Family"; 2001, Altera Version 4.1, pp. 1-17.	
CN	CD	"Mercury, Programmable Logic Device Family"; 2002, Altera Version 2.0, pp. 1-34.	

Examiner Signature	/Chuong Ngo/	Date Considered	02/02/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449A&B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 3 of 3

Complete if Known	
Application Number	10/718,968
Filing Date	November 21, 2003
First Named Inventor	Baeckler
Art Unit	2819
Examiner Name	Not Yet Assigned
Attorney Docket Number	015114-093700US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
CN	CE	"APEX 20K, Programmable Logic Device Family"; 2002, Altera Version 4.3, pp. 1-29.	
	CF	"Stratix FPGA Family"; 2002, Altera Version 3.0, pp. 1-19.	
	CG	"Virtex-II OPlatform FPGAs: Detailed Description"; 2002, Xilinx, Version 2.1.1, pp. 1-40.	
CN	CH	"ORCA Series 2 Field-Programmable Gate Arrays"; 2003, Lattice Semiconductor Corporation, pp. 1-26.	

Examiner Signature	/Chuong Ngo/	Date Considered	02/02/2007

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.